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Representation and minimization of logic functions

DET-03 · Digital Electronics

GUIDING QUESTIONS

- How can a hand-drawn grid of zeros and ones make a logic circuit smaller and cheaper?
- Two circuits look completely different: how can you prove that they do exactly the same job?
- On a cold, sunny day, when should the energy from the photovoltaic (PV) system go into the hot-water tank and when into the lithium iron phosphate (LFP) battery – and how do you turn that rule into a circuit that can be produced efficiently?



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INTENDED LEARNING OUTCOMES

- You synthesize circuits from a description of their function.
- You minimize circuits.
- You assess whether a circuit fulfils the required function.



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AGENDA

1. Combinational logic design
2. Normal forms
3. Algebraic minimization
4. The Karnaugh map
5. Drawing and checking the circuit
6. A complete design
7. What have you learnt?



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REVIEW OF DET-02

- Basic gates NOT, AND and OR; derived operations NAND, NOR, XOR and XNOR
- Seven forms of representation, among them truth table, expression and Karnaugh map
- Boolean algebra: axioms and theorems, among them uniting and De Morgan's laws
- Analysis: from a given circuit to expression, truth table and timing behaviour

Today the other way round: from a description to the smallest circuit

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1 Combinational logic design

Six steps from the description to the circuit: the thread of this lesson

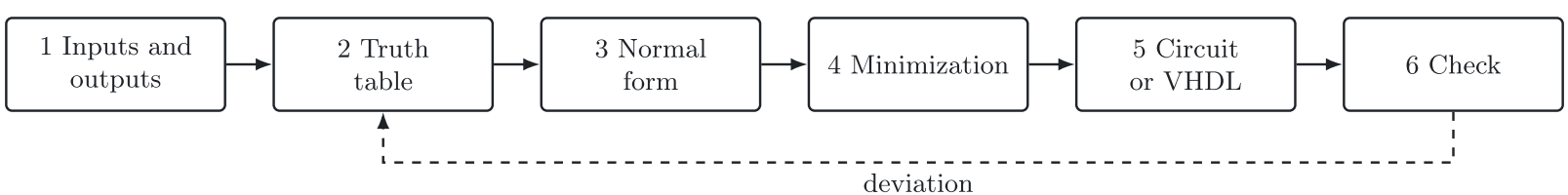
- From analysis to synthesis
- Steps 1 and 2: from the description to the truth table

FROM ANALYSIS TO SYNTHESIS

Synthesis: from the description of a function to the circuit, in six steps

- Step 1: inputs and outputs, each with the meaning of its 1
- Step 2: truth table – decide the output in every row
- Step 3: normal form, read from the truth table
- Step 4: minimization – fewer gates, same function
- Step 5: circuit or VHDL
- Step 6: check against the description – back to step 2 if it deviates

Examples: the ringtone (chapters 1 to 5), a photovoltaic system (chapter 6)



STEPS 1 AND 2: FROM DESCRIPTION TO TRUTH TABLE

Example: when does your smartphone ring audibly?

- Description in words:
  - Silent mode mutes every call
  - Do Not Disturb mutes all calls except those from favourites
  - Silent mode has priority
- Step 1: each variable with the meaning of its 1
  - A: silent mode on
  - B: caller is a favourite
  - C: Do Not Disturb on
  - Y: ringtone audible
- Step 2: decide the output in every row – open questions first
  - Row 7: silent mode wins over the exception for favourites

Row	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	1
4	1	0	0	0
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

2 Normal forms

Step 3: from the truth table to a normal form, an expression of fixed structure

- Minterms
- The disjunctive normal form
- Maxterms
- The conjunctive normal form
- Minterm and maxterm lists

MINTERMS

- Literal: a variable or its negation, A or $\overline{A}$, in a logic expression
  - $\overline{A} \cdot B + \overline{A} \cdot \overline{C}$: three variables, four literals
- Minterm m_i: AND with one literal of each variable, 1 only in row i
  - Variables that are 0 in row i appear negated, the others as they are
  - So all literals are 1 in row i – in every other row, at least one is 0

Example: ringtone

Row i	A	B	C	Y	Minterm m_i
0	0	0	0	1	$\overline{A} \cdot \overline{B} \cdot \overline{C}$
1	0	0	1	0	$\overline{A} \cdot \overline{B} \cdot C$
2	0	1	0	1	$\overline{A} \cdot B \cdot \overline{C}$
3	0	1	1	1	$\overline{A} \cdot B \cdot C$
4	1	0	0	0	$A \cdot \overline{B} \cdot \overline{C}$
5	1	0	1	0	$A \cdot \overline{B} \cdot C$
6	1	1	0	0	$A \cdot B \cdot \overline{C}$
7	1	1	1	0	$A \cdot B \cdot C$

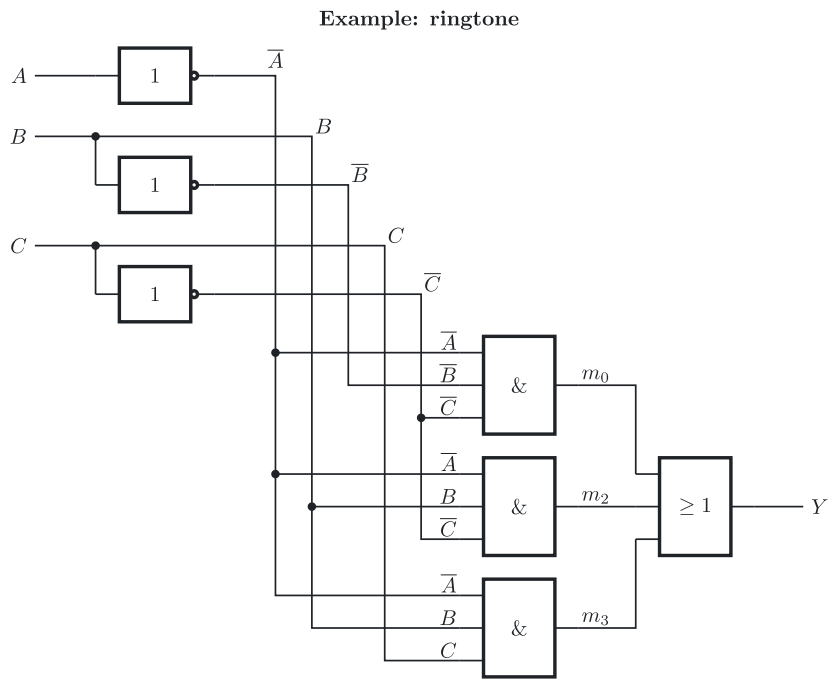
- A: silent mode on, B: caller is a favourite, C: Do Not Disturb on, Y: ringtone audible

THE DISJUNCTIVE NORMAL FORM

- Disjunctive normal form (DNF): OR of AND terms, the product terms
  - Canonical: every term contains every variable
- Canonical DNF: OR of the minterms of all rows with $Y = 1$

$$Y = m_0 + m_2 + m_3$$
$$= \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot C$$

- Two-level circuit: first AND, then OR
- Always correct, but the most gates – chapters 3 and 4 minimize it



MAXTERMS

The same truth table, read from its zeros

- Maxterm M_i: OR with one literal of each variable, 0 only in row i
  - Variables that are 1 in row i appear negated, the others as they are
  - So all literals are 0 in row i – in every other row, at least one is 1

Example: ringtone

Row i	A	B	C	Y	Maxterm M_i
0	0	0	0	1	$A+B+C$
1	0	0	1	0	$A+B+\overline{C}$
2	0	1	0	1	$A+\overline{B}+C$
3	0	1	1	1	$A+\overline{B}+\overline{C}$
4	1	0	0	0	$\overline{A}+B+C$
5	1	0	1	0	$\overline{A}+B+\overline{C}$
6	1	1	0	0	$\overline{A}+\overline{B}+C$
7	1	1	1	0	$\overline{A}+\overline{B}+\overline{C}$

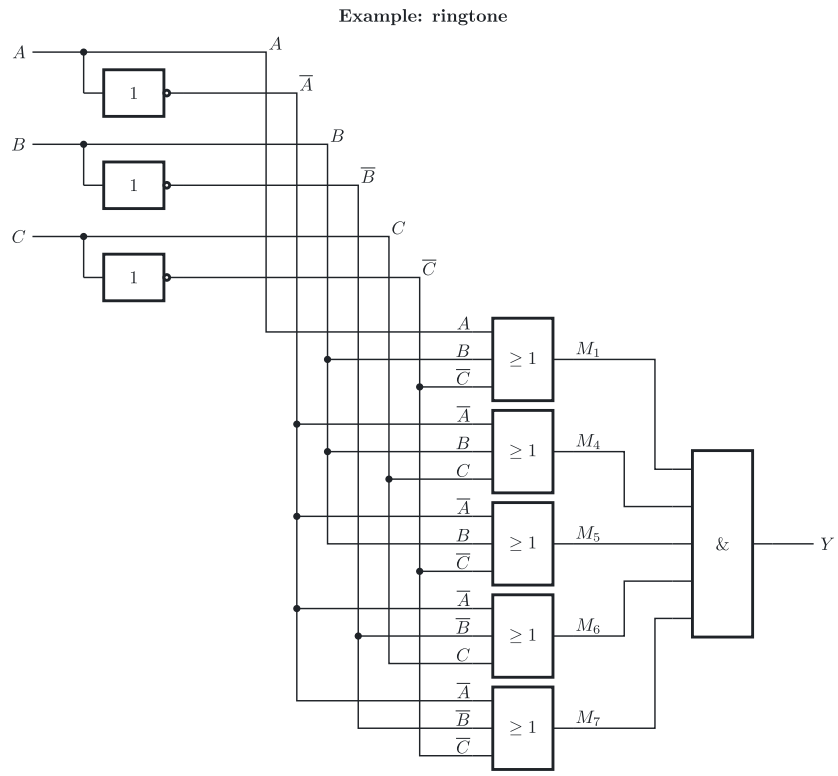
- A: silent mode on, B: caller is a favourite, C: Do Not Disturb on, Y: ringtone audible

THE CONJUNCTIVE NORMAL FORM

- Conjunctive normal form (CNF): AND of OR terms, the sum terms
  - Canonical: every term contains every variable
- Canonical CNF: AND of the maxterms of all rows with $Y = 0$

$$
\begin{aligned}
Y &= M_1 \cdot M_4 \cdot M_5 \cdot M_6 \cdot M_7 \\
&= \left(A + B + \overline{C}\right) \cdot \left(\overline{A} + B + C\right) \\
&\quad \cdot \left(\overline{A} + B + \overline{C}\right) \cdot \left(\overline{A} + \overline{B} + C\right) \\
&\quad \cdot \left(\overline{A} + \overline{B} + \overline{C}\right)
\end{aligned}
$$

- Two-level circuit: first OR, then AND
- The CNF produces the zeros, the DNF the ones



Open in the simulator

MINTERM AND MAXTERM LISTS

- Minterm list: the rows with $Y = 1$; maxterm list: the rows with $Y = 0$
- The variables are named in the order of the truth table

Example: ringtone

$$Y(A, B, C) = \sum m(0, 2, 3)$$

$$Y(A, B, C) = \prod M(1, 4, 5, 6, 7)$$

- m: minterms, M: maxterms, each followed by the numbers of their rows
- Every row number lies in exactly one of the two lists

Two consequences:

- Unique: the same minterm list means the same function
- Few ones: the canonical DNF is shorter; few zeros: the canonical CNF

3 Algebraic minimization

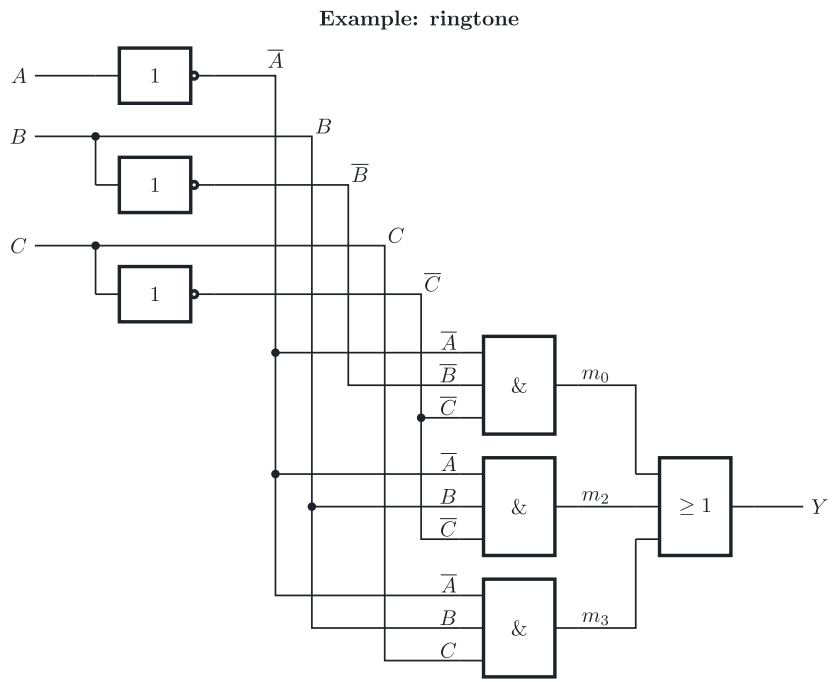
Step 4: fewer gates, same function

- Why minimize?
- The uniting theorem
- Minimizing with the theorems

WHY MINIMIZE?

- Starting point: the canonical DNF of the ringtone – always correct, but expensive
- Minimization: the same function with fewer operations
  - Fewer gates: less area, wiring and power
- Measure of the effort: the gates and their inputs
  - Canonical DNF: four gates with 12 inputs, plus three inverters

Two ways: Boolean algebra (3.2, 3.3) and the Karnaugh map (chapter 4)



THE UNITING THEOREM

- Uniting theorem: two products that differ in only one variable unite into one without it
  - Distributive property, complements and identity, one after the other
- In the ringtone, the minterms m_0 and m_2 differ only in B

$$\begin{aligned}
\overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} &= \overline{A} \cdot \overline{C} \cdot \left(\overline{B} + B\right) && \text{commutative and distributive properties} \\
&= \overline{A} \cdot \overline{C} \cdot 1 && \text{commutative property, complements} \\
&= \overline{A} \cdot \overline{C} && \text{identity}
\end{aligned}$$

- A: silent mode on, B: caller is a favourite, C: Do Not Disturb on
- Meaning: with silent mode and Do Not Disturb off, the phone rings for every caller
  - B has no influence in these two rows, so it drops out

MINIMIZING WITH THE THEOREMS

- In the ringtone, m_2 pairs with m_0 (differs in B) and m_3 (differs in C)
  - Idempotence, $m_2 + m_2 = m_2$, lets us use m_2 twice

$$
\begin{aligned}
Y &= \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot C \\
&= \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot C && \text{idempotence} \\
&= \overline{A} \cdot \overline{C} \cdot \left(\overline{B} + B\right) + \overline{A} \cdot B \cdot \left(\overline{C} + C\right) && \text{commutative and distributive properties} \\
&= \overline{A} \cdot \overline{C} \cdot 1 + \overline{A} \cdot B \cdot 1 && \text{commutative property, complements} \\
&= \overline{A} \cdot \overline{C} + \overline{A} \cdot B && \text{identity} \\
&= \overline{A} \cdot \left(B + \overline{C}\right) && \text{distributive and commutative properties}
\end{aligned}
$$

- Read: the phone rings if silent mode is off and if a favourite calls or Do Not Disturb is off
- Limit: you must spot the pairs yourself – no guarantee of the minimum

4 The Karnaugh map

Step 4 again, now graphically

- Neighbours in the grid
- Loops of ones
- Loops of zeros
- Don't cares
- The chequerboard: XOR

NEIGHBOURS IN THE GRID

- Neighbouring cells differ in exactly one input – their ones unite, as in 3.2
  - Horizontally or vertically, not diagonally
  - Across the edges: left and right, top and bottom
  - Each corner with the corner in its row and the corner in its column
- Labels: where each input is 1; cells: the numbers of their minterms
- Veitch 1952, Karnaugh 1953

	$\overline{B}$	$\overline{B}$	B	B	
$\overline{A}$	0	2	6	4	$\overline{D}$
$\overline{A}$	1	3	7	5	D
A	9	11	15	13	D
A	8	10	14	12	$\overline{D}$
	$\overline{C}$	C	C	$\overline{C}$	

LOOPS OF ONES

- Loops: rectangles of 1, 2, 4, 8 or 16 neighbouring ones, as large as possible
  - Every one in at least one loop; loops may overlap
- Each loop yields a product term
  - Constant 1: as it is; constant 0: negated; changing: drops out
- In the ringtone, the loop on the right gives $\overline{A} \cdot B$, the loop across the edges $\overline{A} \cdot \overline{C}$

$$Y = \overline{A} \cdot B + \overline{A} \cdot \overline{C}$$

Example: ringtone

	$\overline{B}$	$\overline{B}$	B	B
$\overline{A}$	1	0	1	1
A	0	0	0	0
	$\overline{C}$	C	C	$\overline{C}$

- A: silent mode on, B: caller is a favourite, C: Do Not Disturb on

LOOPS OF ZEROS

- Loops of zeros yield the sum terms of a minimized CNF
  - Reversed, as for maxterms: constant 1 negated, constant 0 as it is
- In the ringtone, the lower row gives $\overline{A}$, the second column $B + \overline{C}$

$$Y = \overline{A} \cdot \left(B + \overline{C}\right)$$

- The last line of 3.3, found directly – here cheaper than the DNF of the ones

Example: ringtone

	$\overline{B}$	$\overline{B}$	B	B
$\overline{A}$	1	0	1	1
A	0	0	0	0
	$\overline{C}$	C	C	$\overline{C}$

DON'T CARES

- Don't care X: the output does not matter – treat it as 1 or 0, whichever gives larger loops
  - Only if the combination really never occurs or its output does not matter
- Example: 0 to 4 signal bars as a number with three bits; Y: at least three bars
  - The codes 5 to 7 never occur: don't cares d

$$Y(A,B,C) = \sum m(3,4) + d(5,6,7)$$

$$Y = A + B \cdot C$$

Example: at least three bars

	$\overline{B}$	$\overline{B}$	B	B
$\overline{A}$	0	0	1	0
A	1	X	X	X
	$\overline{C}$	C	C	$\overline{C}$

THE CHEQUERBOARD: XOR

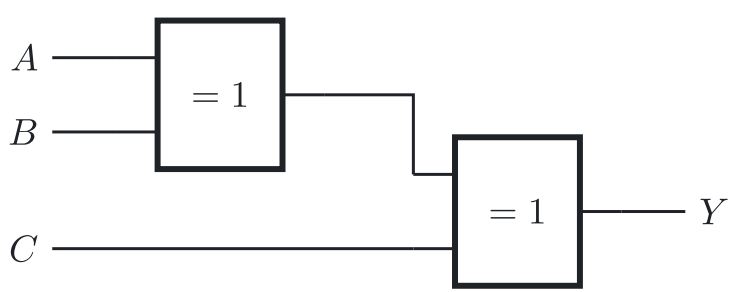
- Intermediate switching: each of the switches A, B and C toggles the light Y
- Its map is a chequerboard: no two ones are neighbours, no loop unites them
- The chequerboard reveals XOR, with $Y = 1$ for an odd number of ones:

$$Y = A \oplus B \oplus C = (A \oplus B) \oplus C$$

- Two XOR gates with two inputs replace the canonical DNF

Example: staircase light

	$\overline{B}$	$\overline{B}$	B	B
$\overline{A}$	0	1	0	1
A	1	0	1	0
	$\overline{C}$	C	C	$\overline{C}$



5 Drawing and checking the circuit

Steps 5 and 6: from the minimized expression to the checked circuit

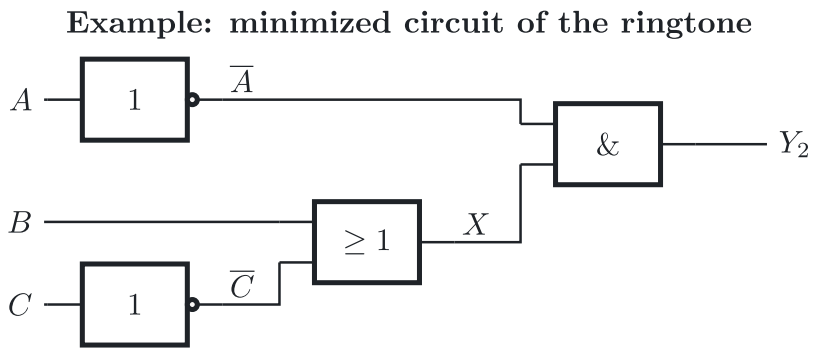
- Step 5: from the expression to the circuit
- Two circuits, one function?
- Does the circuit do what it should?

STEP 5: FROM EXPRESSION TO CIRCUIT

- A minimized DNF or CNF becomes a two-level circuit directly

$$X = B + \overline{C}$$
$$Y_2 = \overline{A} \cdot X = \overline{A} \cdot \left(B + \overline{C}\right)$$

- A: silent mode on, B: caller is a favourite, C: Do Not Disturb on
- An OR gate forms the intermediate node X, an AND gate combines it with $\overline{A}$
- Effort: two gates with four inputs instead of four with 12 – if it does the same job



TWO CIRCUITS, ONE FUNCTION?

Does the minimized circuit Y_2 do the same job as the canonical DNF Y_1?

$$Y_1 = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot C$$

$$Y_2 = \overline{A} \cdot \left(B + \overline{C}\right)$$

Three ways to prove it:

1. Truth tables: Y_1 and Y_2 agree in every row
2. Minterm lists: both are $\sum m(0, 2, 3)$
3. Boolean algebra: section 3.3 turns Y_1 into Y_2

Example: ringtone

A	B	C	$X = B + \overline{C}$	$Y_2 = \overline{A} \cdot X$	Y_1
0	0	0	1	1	1
0	0	1	0	0	0
0	1	0	1	1	1
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	0	0	0
1	1	0	1	0	0
1	1	1	1	0	0

Open in the simulator

DOES THE CIRCUIT DO WHAT IT SHOULD?

- A circuit fulfils the function only if every row agrees with the description
  - A single deviating row, a counterexample, is enough to reject it
- A third design, Y_3, compared with the minterm list of the ringtone:

$$Y_3 = \overline{A} \cdot \overline{C} = \sum m(0,2) \neq \sum m(0,2,3)$$

- A: silent mode on, B: caller is a favourite, C: Do Not Disturb on
- Counterexample, row 3: silent mode off, Do Not Disturb on, a favourite calls – the phone stays silent
  - The term $\overline{A} \cdot B$, which lets the favourites through, is missing
- Look closely at exceptions; clarify open rows first

6 A complete design

All six steps for the PV surplus, from the rule to the checked circuit

- The rule and its truth table
- Minimizing both outputs
- VHDL, simulation and check

THE RULE AND ITS TRUTH TABLE

Example: photovoltaic (PV) surplus

- Rule: the battery first, up to 80 %; then the hot water, unless it is hot enough or the sun heats it
- Step 1, inputs and outputs:
  - A: PV surplus
  - B: battery at least 80 %
  - C: hot water below its upper set point
  - D: solar thermal pump on
  - Y: surplus into the hot water
  - Z: surplus into the battery
- Step 2: the truth table

Row	A	B	C	D	Y	Z
0	0	0	0	0	0	0
1	0	0	0	1	0	0
2	0	0	1	0	0	0
3	0	0	1	1	0	0
4	0	1	0	0	0	0
5	0	1	0	1	0	0
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	1
9	1	0	0	1	0	1
10	1	0	1	0	0	1
11	1	0	1	1	0	1
12	1	1	0	0	0	1
13	1	1	0	1	0	1
14	1	1	1	0	1	0
15	1	1	1	1	0	1

MINIMIZING BOTH OUTPUTS

Steps 3 and 4: from the truth table to the minimized expressions

- Z, loops of ones: $Z = A \cdot \overline{B} + A \cdot \overline{C} + A \cdot D$
- Z, loops of zeros – shorter: $Z = A \cdot \left(\overline{B} + \overline{C} + D\right)$
- Y is a minterm; shared gate $X = B \cdot C \cdot \overline{D}$: $Y = A \cdot X$, $Z = A \cdot \overline{X}$

Example: PV surplus

Loops of ones

	$\overline{B}$	$\overline{B}$	B	B	
$\overline{A}$	0	0	0	0	$\overline{D}$
$\overline{A}$	0	0	0	0	D
A	1	1	1	1	D
A	1	1	0	1	$\overline{D}$
	$\overline{C}$	C	C	$\overline{C}$	

Loops of zeros

	$\overline{B}$	$\overline{B}$	B	B	
$\overline{A}$	0	0	0	0	$\overline{D}$
$\overline{A}$	0	0	0	0	D
A	1	1	1	1	D
A	1	1	0	1	$\overline{D}$
	$\overline{C}$	C	C	$\overline{C}$	

VHDL, SIMULATION AND CHECK

- Step 5, VHDL: X becomes a signal
- Step 6, check: without a surplus both outputs 0, with a surplus exactly one 1

Large functions: tools minimize; how a computer does it: DET-04

Open in the simulator

```
-- A: PV surplus, B: battery at 80 % or more
-- C: below upper set point
-- D: solar thermal pump on
-- Y: into the hot water, Z: into the battery
entity pv_surplus is
  port (A, B, C, D : in  bit;
        Y, Z       : out bit);
end entity;

architecture behaviour of pv_surplus is
  signal X : bit;  -- hot water takes the surplus
begin
  X <= B and C and not D;
  Y <= A and X;
  Z <= A and not X;
end architecture;
```

7 What have you learnt?

- The building blocks of knowledge
- Answers to the guiding questions

WHAT YOU HAVE LEARNT

- Representation of logic functions (normal forms)
- Algebraic minimization
- Minimization with the Karnaugh map

ANSWERS TO THE GUIDING QUESTIONS

- Karnaugh map: neighbouring ones unite – fewer gates and gate inputs
- Same job: the same truth table or the same minterm list
- Hot water only with a surplus, the battery at 80 % or more, room in the tank and the solar thermal pump off – otherwise the battery
  - Truth table, Karnaugh map and a shared term: three AND gates and two inverters



Image by Qwen-Image 2.1

Your turn: first on your own, then together.